EE 4250   **Digital Integrated Circuits**   **Spring 2007**

Catalog Description: Prereq.: EE 3220, 3221, and 3232. 2 hrs. lecture; 2 hrs. lab. ABET category: 2 hrs. design; 1 hr. engineering science. Analysis and design of digital integrated circuit logic gates in bipolar and MOS technology; semiconductor memories and their operations.

Instructor: Dr. Dooyoung Hah, 229 EE Building. Ph: 578-5532. dyhah@lsu.edu
Lecture: MW 8:40 – 9:30 AM, 225 TUREAUD HALL
Office Hours: MW 9:40 – 11:40 AM, T 10:40 – 11:40 AM, other times by appointment only
Course Homepage: http://www.ece.lsu.edu/dyhah/EE4250_spring2007/EE4250_spring2007.html
Textbook: Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology, D. A. Hodges, H. G. Jackson and R. A. Saleh, McGraw-Hill, 3rd Edition, 2003.

Topics Covered: (* Not all topics may be covered. Additional materials may be added.)
- ✓ Introduction
- ✓ Bipolar transistor logics
- ✓ MOS transistor
- ✓ MOS transistor fabrication
- ✓ MOS inverter circuits
- ✓ Static MOS gate circuits
- ✓ High-speed CMOS logic design
- ✓ Transfer gate and dynamic logic design
- ✓ Semiconductor memory design

Grading Policy: Your final grade is based on accumulation of followings.

✓ Home assignments	10%		
✓ Pop-quizzes	5%		
✓ Laboratory	20%		
✓ Test1 (in-lecture)	20%	(Feb. 12, Mon., in-lecture)	
✓ Test2 (in-lecture)	20%	(Mar. 26, Mon. in-lecture)	
✓ Final exam	<u>25%</u>	(May 7, Mon., 3-5pm)	
	100%		

* Final letter grades: absolute + relative performances.

* Different scales will be used for letter grades between graduate students and undergraduate students.

Regrade Policy:

All questions regarding the grading of any assignment/exam (other than points being added incorrectly) are handled *exclusively* through _written_ request and will _only_ be accepted within the first week after grading is completed, announced in class and the assignment is made available. To submit a regrade request, print/type your name on a separate sheet of paper and include a concise explanation of all your concerns/questions and JUSTIFY why you think you deserve additional credit. _Staple_ this sheet to the front of your graded assignment/exam and resubmit it to your instructor during office hours. The assignment will be regraded in its entirety and returned to you. If you continue to have concerns, arrange for an appointment with your instructor to discuss the issue.

Examinations / Quizzes / Homeworks:

Examinations are given in lecture on the dates indicated above. Schedule conflicts must be resolved prior to the exam date and NO makeup exams are given. All exams will be closed book, closed notes. A one-page formula sheet may be allowed. Calculators may or may not be allowed depending on the examination content (i.e. learn to think without them!). When allowed, calculators may only be used for simple algebraic and trigonomentric operations (i.e. no programmable features). A comprehensive final exam will be given during finals week.

A few pop-quizzes will be given throughout the semester either in the beginning or at the end of a lecture without notice.

Late homework will not receive any credit.

General Class Procedures and Office Hours:

Students are responsible for all announcements made in lecture. Course information, announcements and grades will also typically be posted on the course website. It is a sound practice to check the website periodically for important updates and information you may have missed.

Assistance is available from the instructor during office hours; however, do not expect the staff to do your homework for you! Carefully prepare your questions beforehand and answer as many of them as possible for yourself. Please observe the posted office hours for this course and confine your visits to those time slots. If the posted hours conflict with your schedule, you can make an appointment and alternate arrangements will be made to accommodate you.

LEARN TO USE ELECTRONIC MAIL (E-MAIL)! You are encouraged to use your PAWS computer account and electronic mail as this is a great way to communicate with your instructor for this course. Students NOT using the PAWS account should have it set to forward all campus correspondence.

EE 4250 Laboratory   Digital Integrated Circuits   Spring 2007

Instructor: Dr. Dooyoung Hah (dyhah@lsu.edu) – Section 1, T 8:40 – 10:30 am

                Office hour: MW 9:40 – 11:40 AM, T 10:40 – 11:40 AM

           Mr. Siva Yellampalli (syella1@lsu.edu) – Section 2, T 3:40 – 5:30 pm

             Office hour:

Lab Instruction: Handouts

Lab Schedule:

- ✓ Lab#0 (1/23): Laboratory instrumentation
- ✓ Lab#1 (1/30): Bipolar transistor inverter
- ✓ Lab#2 (2/6): Voltage transfer characteristics of TTL gates
- ✓ Lab#3 (2/13): MOS transistor *I-V* characteristics
- ✓ Lab#4 (2/27): Voltage transfer characteristics of MOS inverters
- ✓ Lab#5 (3/6): Noise in a CMOS inverter chain
- ✓ Lab#6 (3/13): CMOS NAND and NOR gate characteristics
- ✓ Lab#7 (3/20): CMOS flip-flops (I)
- ✓ Lab#8 (3/27): CMOS flip-flops (II)
- ✓ Design project (4/10): Static MOS gate circuits
- ✓ Lab#9 (4/17): TTL and CMOS gates delay
- ✓ Lab#10 (4/24): MOS pass gates and T-gate
- ✓ Lab#11 (5/1): Makeup lab

      * The schedule above is tentative and may be changed if necessary.

General Grading Policy:

- ✓ Perfect score for each lab session is 10 points.
- ✓ Unreasonable discussion or illogical data interpretation → " – 1"
- ✓ Lack of discussion or data interpretation → " – 2"
- ✓ Unreasonable experiment results → " – 1" to " – 2"
- ✓ Unreasonable SPICE simulation results → " – 1"
- ✓ Lack of SPICE simulation results → " – 2"
- ✓ Late reports → " – 1" per week
- ✓ "0" is the minimum score.
- ✓ Missing lab: "0" point.

Notes: 1. You should be ready for each lab before you come. This includes …

             - To read and to understand the lab instruction before each lab session

- **To perform SPICE simulation and to bring the results**
- To complete reports for the previous lab before the new lab session starts
- To show up on time

2. For each lab except the Lab#0, a report must be submitted to the instructor on the following lab session before the session starts. Every student (**not every group!**) must compose a report. Each report can be organized as following:

    a. Objective

    b. Circuit diagram

    c. Experimental observations

    d. Interpretation of the data, discussion, difficulties, etc.

Other tips:

- It is discouraged to simply copy the theory to the reports. Additional theoretical backgrounds or discussion, on the other hand, is welcomed.
- Some lab sessions require SPICE simulation. If a session demands to do so, the results must be brought for the session and submitted after the session is finished.
- Write the name of your lab partner on the cover page.

3. Laboratory etiquettes

- Take a good care of the lab instruments. If you are not sure what you are doing, it is better to ask than to *go for it*.
- Do not eat or drink in the lab.
- Clean your table as much as you can before you leave the lab. That includes returning of the components to their original locations and turning off the instruments.

4. Useful tips

- Circuit connection: try to be neat and shorten the wiring. Messy wiring is not only easy to cause an error but also hard to debug. Use a color of wire as an indication. For example, red wires for positive voltage supply, blue wires for negative voltage supply, black wires for ground, green wires for signal, etc.
- It has been brought to the instructor's attention that some parts of some breadboards have defects. Also some active devices such as transistors, diodes, logic gates, etc, might not be working. If you suspect such things, move your circuit to other part of the breadboard or replace the suspicious components.

- If you feel there is no progress for long time, ask for help from the instructor. Don't wait until the last minute.
- If you have an *inevitable* need to miss a lab session, contact the instructor as early as possible so that proper arrangement can be made. For example, medical emergency, family emergency, and job interview, are reasonable reasons.